



UVDM40SC

DC to 40 GHz MMIC Medium Power Voltage Controlled Attenuator

Data Sheet

Application

The UVDM40SC MMIC voltage controlled attenuator is ideal for high frequency and broadband applications in test equipment, commercial and military systems. The attenuator is especially suited for applications needing a moderate amount of adjustable attenuation and fast attenuation control from DC to millimeter frequencies. The device is also useful as a general purpose building block in communications systems.

Description

The UVDM40SC is a medium-power DC-40 GHz PHEMT FET attenuator. The performance of the device is controlled by two bias voltages, V_{series} and V_{shunt} . The bias voltages control the match and attenuation of the device when varied between -1V and +0.5V DC. Please refer to the tables of recommended bias settings optimized for flat insertion loss and flat attenuation for additional information.

Features

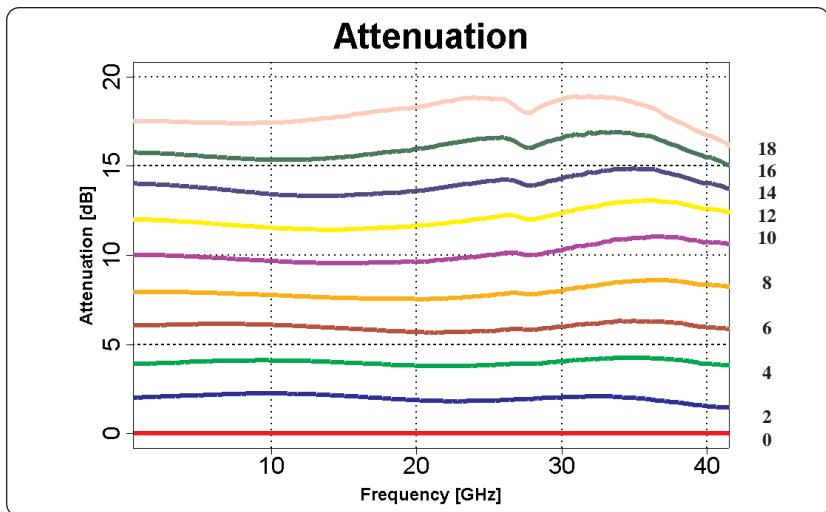
- Wideband operation: DC to 40 GHz
- Low Insertion Loss (<3 dB)
- Good Input/Output Match
- Medium Attenuation (max. 18 dB)
- Size: 1640 x 920 μm

Key Specifications

$Z_0=50 \Omega$

Parameter	Description	Minimum	Typical	Maximum
Attenuation (dB)	DC to 40 GHz	0	—	18
Flatness (\pm dB)	DC to 40 GHz	—	1.0	—
Insertion Loss (dB)	DC to 40 GHz	3	—	20
S11 (dB)	DC to 50 GHz	—	-10	-8
S22 (dB)	DC to 50 GHz	—	-10	-8
P_{-1dB} (dBm)	1dB Gain Compression 0 to 15 dB Attenuation	—	12	—

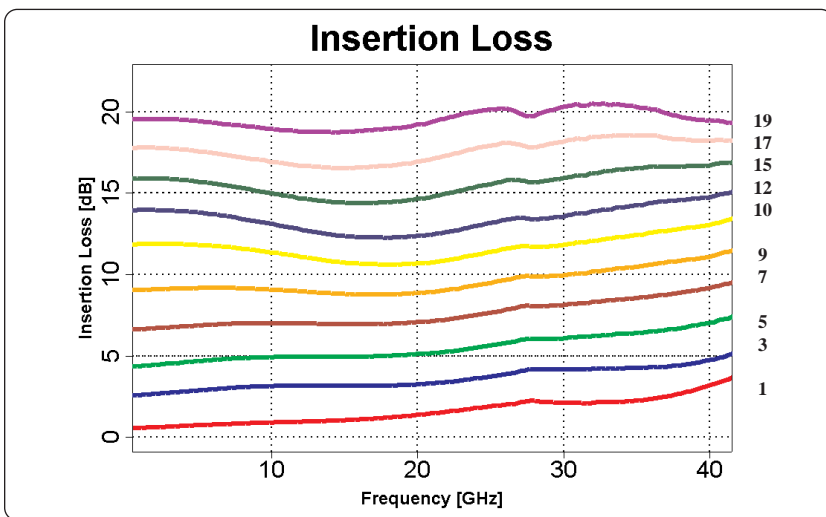
Optimized for Flat Attenuation (Typical)



V_{series} (V)	V_{shunt} (V)	Att. (dB)*
-0.625	0.343	18.3
-0.625	-0.287	15.9
-0.625	-0.400	13.6
-0.616	-0.456	11.6
-0.608	-0.501	9.6
-0.601	-0.544	7.5
-0.595	-0.583	5.7
-0.569	-0.622	3.8
-0.550	-0.700	1.8
0.500	-1.000	0

Figure 1: Typical on wafer measured performance.

Optimized for Flat Insertion Loss (Typical)



V_{series} (V)	V_{shunt} (V)	Loss (dB)*
-0.650	0.000	19.2
-0.650	-0.312	16.9
-0.650	-0.413	14.6
-0.650	-0.475	12.4
-0.641	-0.513	10.7
-0.618	-0.549	8.9
0.595	-0.583	7.1
-0.568	-0.624	5.1
-0.550	-0.700	3.3
0.500	-1.000	1.4

Figure 2: Typical on wafer measured performance.

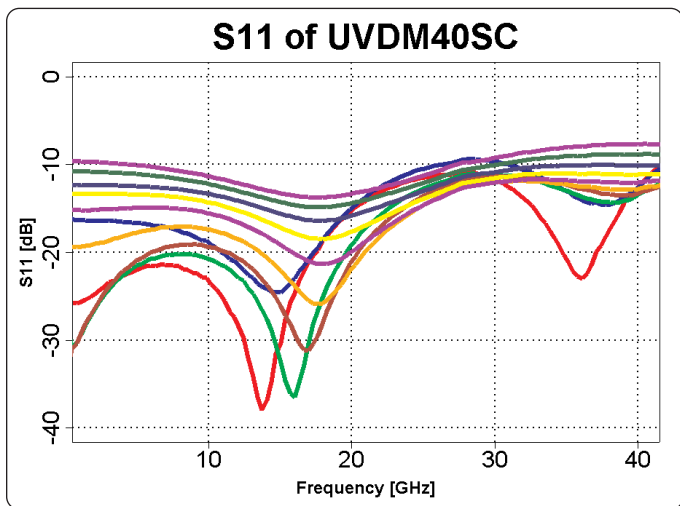


Figure 3: Typical on wafer measured performance.

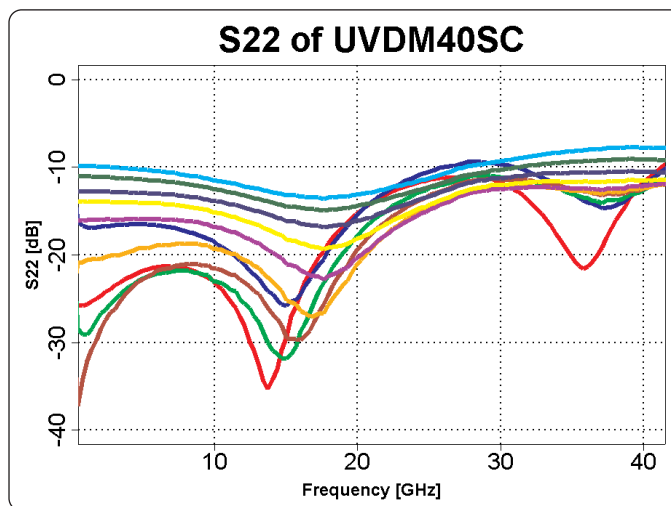


Figure 4: Typical on wafer measured performance.

Note: S-parameter measurement files are available upon request. Email: support@centellax.com for more information.

(*) Midband

Supplemental Specifications

CENTELLAX



SPEED INNOVATION

Parameter	Description	Minimum	Typical	Maximum
V_{series}	Attenuation Control Voltage	-2 V	—	0.5 V
V_{shunt}	Attenuation Control Voltage	-2 V	—	0.5 V
DC_{in}	DC feedback circuit input	0 V	0.25 V	1 V
DC_{out}	DC feedback circuit output	0 V	0.25 V	1 V
GND	Backside Ground Plane			
Tch	Channel Temperature	—	—	150°C
Θ_{ch}	Thermal Resistance ($T_{case}=25^{\circ}C$)	—	60°C/Watt	—

Pick up and Chip Handling:

The chip has exposed air bridges on the top surface. Do not pick up chip with vacuum on the die center; handle at edges or with a custom collet.

ESD Handling and Bonding:

This MMIC is ESD sensitive and preventive measures should be taken during handling, die attach and bonding.

Epoxy die attach is recommended.

Please visit our website for more handling, die attach and bonding information.

(www.centellax.com)

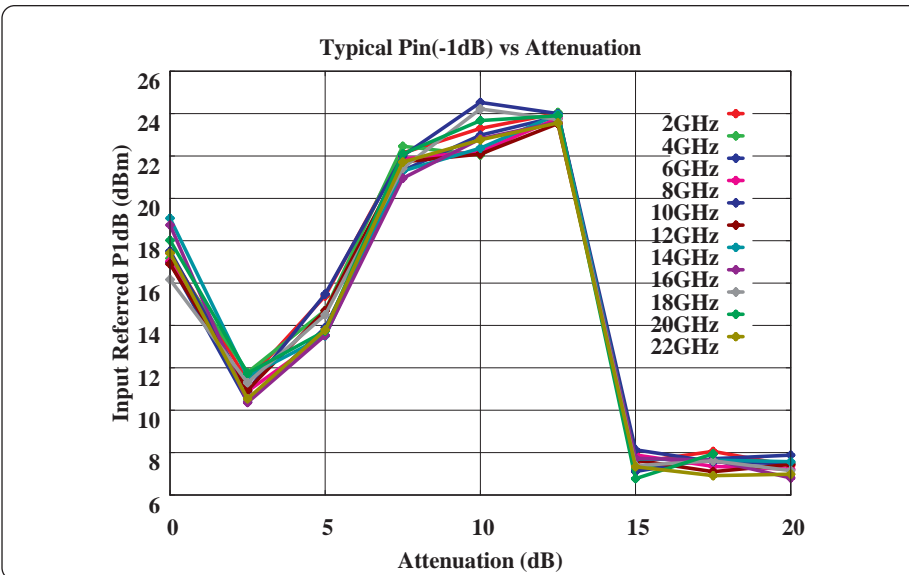


Figure 5: Typical on evaluated package measured performance.

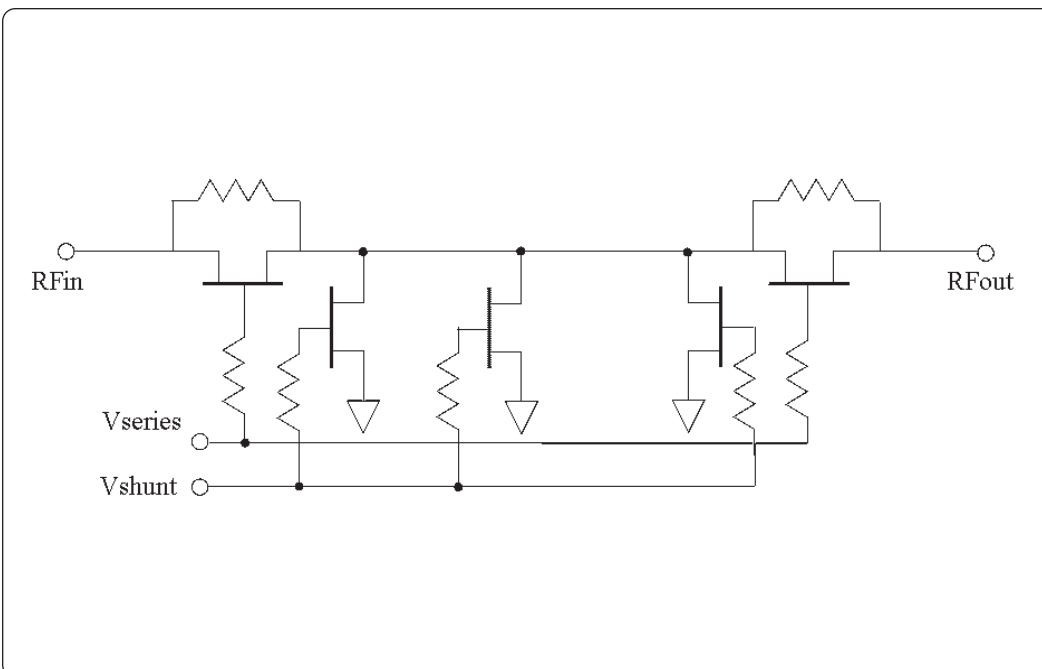


Figure 6: UVDM40SC Simplified Schematic Diagram

DC Feedback Circuit for Variable Attenuator

The following feedback circuit does a good job of providing the series and shunt biases to the variable attenuator for a user-selected amount of attenuation.

The circuit references a 1/3 scale version of the microwave attenuator, which is used for the DC feedback loop. Because the devices are 1/3 the size of the unscaled attenuator, the reference impedance is 3 times larger (150Ω instead of 50Ω).

The circuit uses two ordinary opamps to provide the bias control voltages to the attenuator. Opamp **OA1** senses the input impedance

of the attenuator and adjusts the series FET gate voltage V_{series} so that the impedance looking into the attenuator is 150Ω. The input impedance can be adjusted with the potentiometer shown in the schematic (Figure 7). When this feedback loop is at DC equilibrium the voltage at DC_{in} will be $V_{ref}/2$.

The second opamp **OA2** adjusts the shunt FET gate voltage so that the DC output voltage DC_{out} is equal to the voltage at the opamp negative input terminal. When 0V is applied to the negative input terminal of **OA2**, the attenuation is maximized.

Conversely, if $V_{ref}/2$ is applied at

the negative input of **OA2** then the attenuation is minimized.

A voltage divider with the shunt resistor terminated by the voltage V_{ref} makes for a convenient conversion of voltage to attenuation. If the input to the divider V_{atten} is set to 0 volts then the negative input of **OA2** will have a value of $V_{ref}/2$ and the attenuator will have minimum attenuation.

Conversely, if V_{atten} is set to $-V_{ref}$ then the negative input of **OA2** is set 0V and the attenuator will have maximum attenuation. This makes the calculation of V_{atten} easy and requires a minimum number of parts.

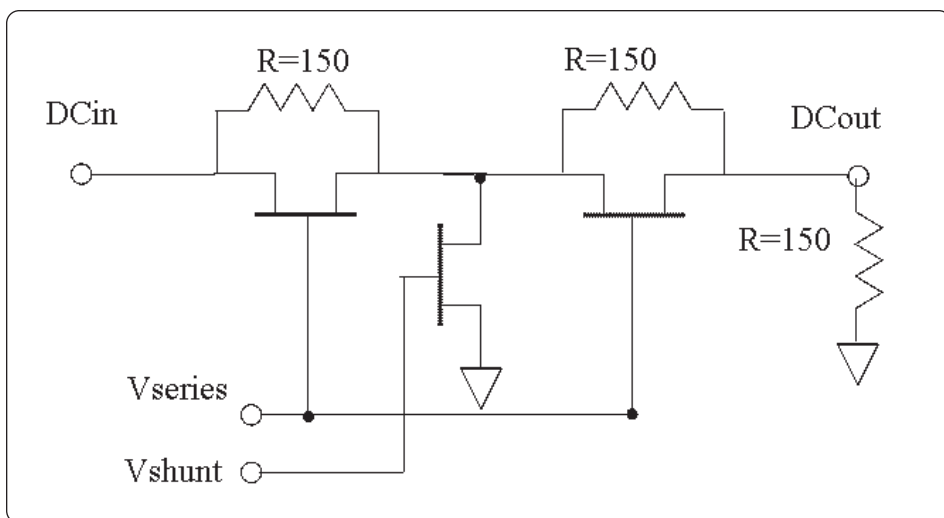


Figure 7: Scaled DC Attenuator Circuit (1/3 scale attenuator)

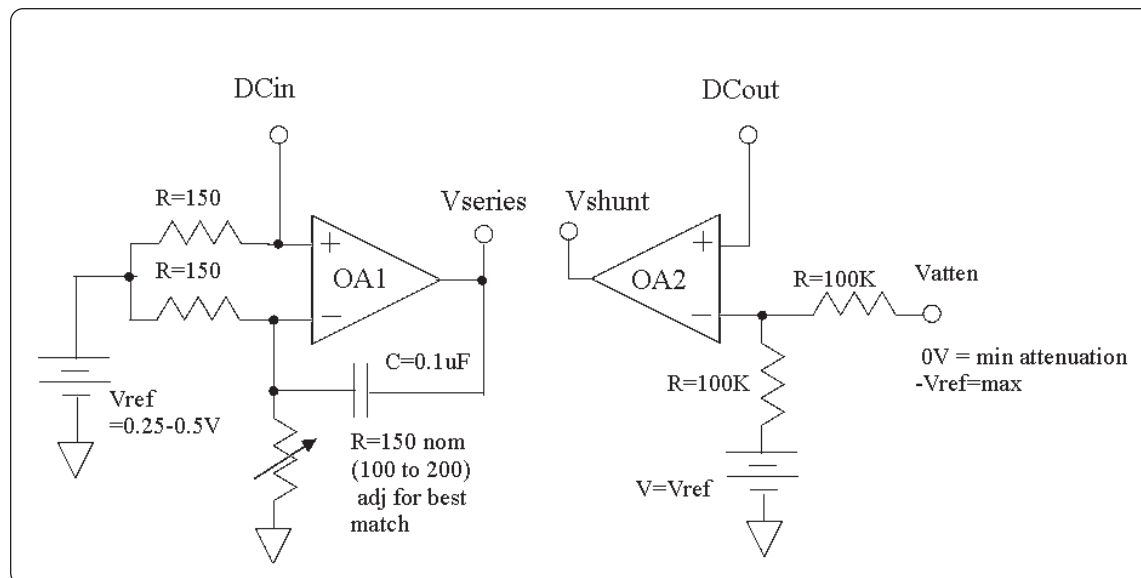
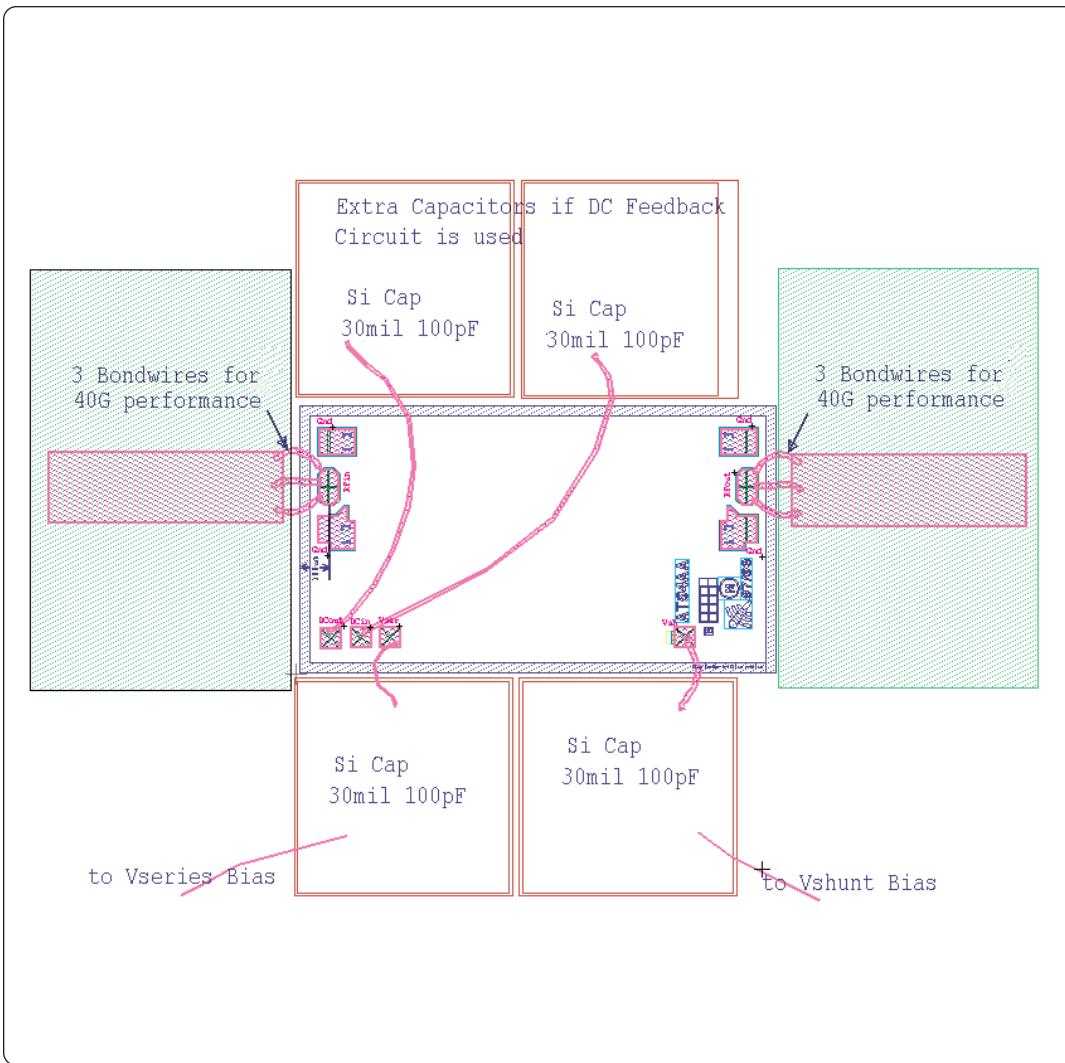


Figure 8: The DC feedback circuit to adjust the attenuator



Assembly Diagram of UVDM40SC



Physical Characteristics of UVDM40SC

